



## Service Information





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## 1. GENERAL MAINTENANCE INFORMATION

### 1-1. INTRODUCTION

Atari video games consist of a cabinet, TV monitor, a printed circuit board (PCB) computer, interconnecting wiring, and various cabinet-mounted circuit components. Except for a schematic, no information about the TV monitor is presented in this manual. The TV monitor is a Motorola XM701 unit. TV circuit malfunctions can be solved using standard TV troubleshooting techniques. However, the PCB computer requires troubleshooting techniques that may be unfamiliar to the average technician. Therefore, the troubleshooting information in the manual is dedicated to the PCB computer and its associated cabinet circuitry.

### 1-2. WARRANTY

This game has been designed with solid state circuitry to be as maintenance-free as possible. However, as with all devices mechanical or electrical, there may be minor problems. If the printed circuit board (PCB) fails within the 90-day\* warranty period, contact the distributor from whom the game was originally purchased for replacement or repair instructions. All such warranty returns must be accompanied by completed warranty return forms. Any PCB repairs attempted by anyone other than authorized Atari Service Center personnel will void the warranty. If the PCB fails after the warranty period has expired, it will be repaired for a nominal parts and labor charge.

Atari, Inc. warrants the T.V. monitor for a period of 30 days commencing the day of shipment from the Atari factory. If the monitor fails within that period, immediately contact the distributor from whom the game was originally purchased for repair or replacement instructions. Any T.V. repairs (other than replacement of fuses or adjustments) attempted during the warranty period by anyone other than authorized Atari Service Center personnel will void the warranty.

\*(From date of shipment from the factory)

If the T.V. monitor fails after the warranty period has expired, it may be returned to the distributor where it will be repaired for a nominal parts and labor charge, or it may be taken to any competent TV repair shop.

### 1-3. NEW MACHINE SET-UP PROCEDURE

Before turning this machine on, inspect it carefully for any damage which may have occurred during shipment. Inspect both interior and exterior of the machine for any obvious damage to the cabinet or internal components. Check for cracked or broken cabinet parts, assemblies pulling loose, broken or disconnected wires of foreign objects shorting electrical connections. After the machine has been plugged in and turned on, perform the checkout procedure.

### 1-4. NEW MACHINE CHECKOUT

As each new machine leaves the factory, every component and subassembly is carefully checked for proper operation. However, since parts may have been damaged or adjustments changed during shipping, the following checkout procedure must be repeated prior to placing the machine on location:

1. Inspect both the exterior and interior of the machine for obvious shipping damage such as cracked or broken cabinet parts, subassemblies broken loose, etc.
2. Carefully inspect the interior of the machine to see that all solder joints, slip-on connectors and plug-in type connectors are firmly seated. Pay particular attention to the PCB edge connector, the fuses and any connectors to the potentiometers. Also check the connections to the coin switch, the T.V. monitor, the interlock switches and all the other Molex-type connectors.
3. Plug the machine in, and pull out the white actuator shafts of the interlock switches if the rear door is open. Inspect the CRT (cathode ray tube) image for a steady and sharp picture which exhibits the proper levels of brightness and contrast.
4. Insert several old and new coins into the coin acceptor. No genuine coin should be rejected and each coin insertion should step the coin counter one digit. Depress the coin rejector button to make sure that the linkage is operating smoothly.



5. Coin insertion should start the game. Check for proper game sequence, making sure that all aspects of the game are functioning correctly.
6. The door locks should turn to the "locked" and "unlocked" positions smoothly and the doors should open and close without binding.
7. The interlock switches must turn off the entire machine when the rear door is opened.

#### 1-5. TV ADJUSTMENT

- The adjustment of the TV monitor functions like that of a normal TV set. The only exception to that is the audio portion of the TV is not used. The volume control is located on the PC computer Board. The monitor is adjusted through the rear door.
- a. Brightness: Adjust the brightness before the contrast. Adjust so that the CRT background is as dark as possible.
  - b. Contrast: The contrast is adjusted so that the images displayed on the CRT are as bright and clear as possible without being blurred.
  - c. Vertical Hold: The vertical hold should only be adjusted if the picture is rolling up or down the screen. Adjust for a stable centered picture.
  - c. Horizontal Hold: If the picture is slightly off center horizontally, if the images appear warped or if the picture is broken into a series of diagonal lines, adjust the H Hold.
  - e. Vertical Size: Adjust only if the top and bottom of the race course is cut off from the visible portion of the screen or there is too much distance between the edge of the course and the edge of the screen which will appear as an extra set of horizontal dotted lines on the top and bottom of the CRT display. Adjust for maximum picture size.
  - f. Vertical Linearity - Change this adjustment only if the top of the picture seems compressed.

- g. The Yoke - The yoke should never need adjustment unless the adjuster has been tampered or damaged. If yoke adjustment is necessary, both yoke rings should be rotated simultaneously for optimum centering of the picture on the CRT.

1-6. Q-530 COIN ACCEPTOR: OPERATION, ADJUSTMENT & MAINTENANCE

All coin acceptors leave the factory adjusted for maximum performance. If, however, more critical adjustments are desired, or if the unit has been completely disassembled for service, the following adjustment procedure is suggested. If the coin acceptor has been removed from the machine, place it in a vertical position on a level surface. If the acceptor is still mounted on the coin door, place the coin door in a vertical position on a level surface.

a. Kicker and Separator

1. Set the acceptor with the back of the unit facing you in the test position.
2. Loosen the screws holding the kicker (1) and the separator (3) and move both the kicker (2) and the separator (4) as far to the right as they will go. Tighten the screws.
3. Insert several test coins (both old and new) and note that some are returned by striking the separator.
4. Loosen the separator screw and move the separator a slight amount to the left. Tighten the screw.
5. Insert the test coins again and, if some of them are still returned, repeat Step 4 until all the coins are accepted.
6. Loosen the kicker screw and move the locker as far to the left as it will go. Tighten the screw.
7. Insert the test coins and note that some are returned.
8. Loosen the kicker screw and move the kicker a slight amount to the right. Tighten the screw.
9. Insert the coins again and, if some are still returned, repeat Step 8 until all the coins are accepted.
10. Be sure that both screws are tight after the adjustments have been made.

b. The Magnet Gate

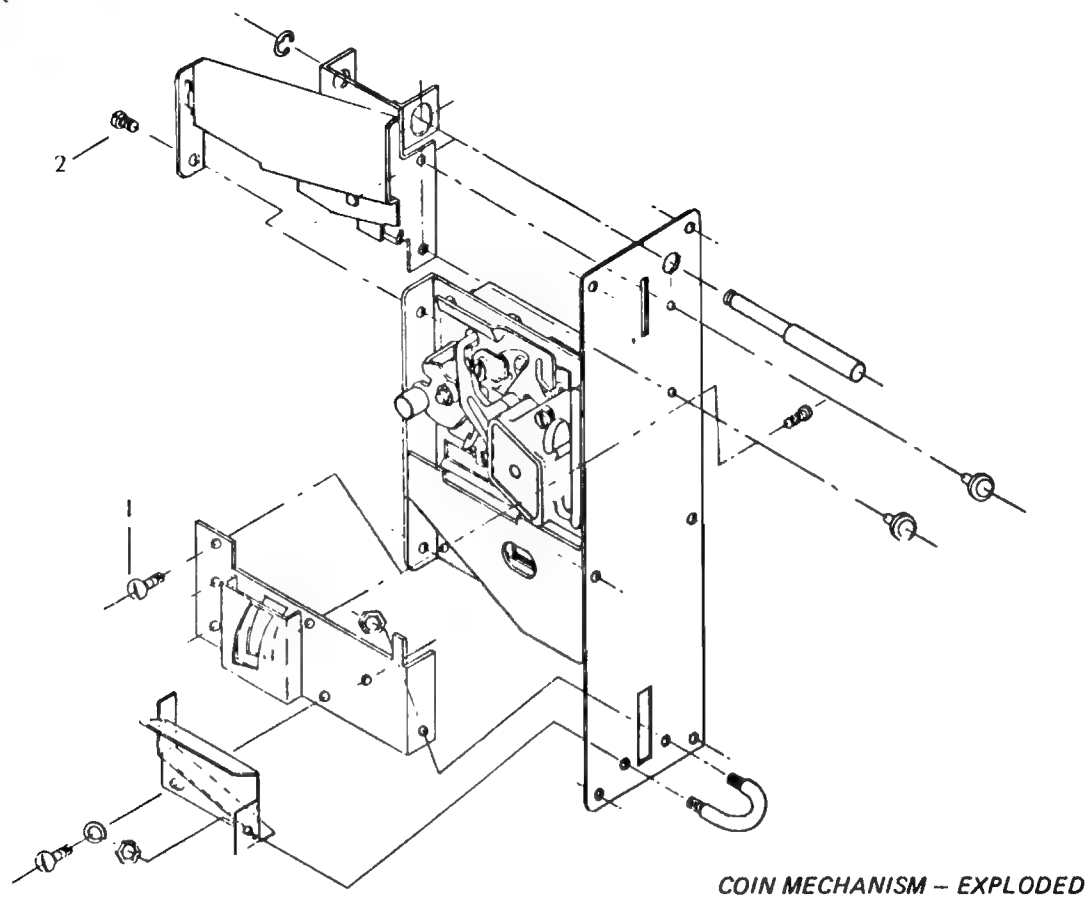
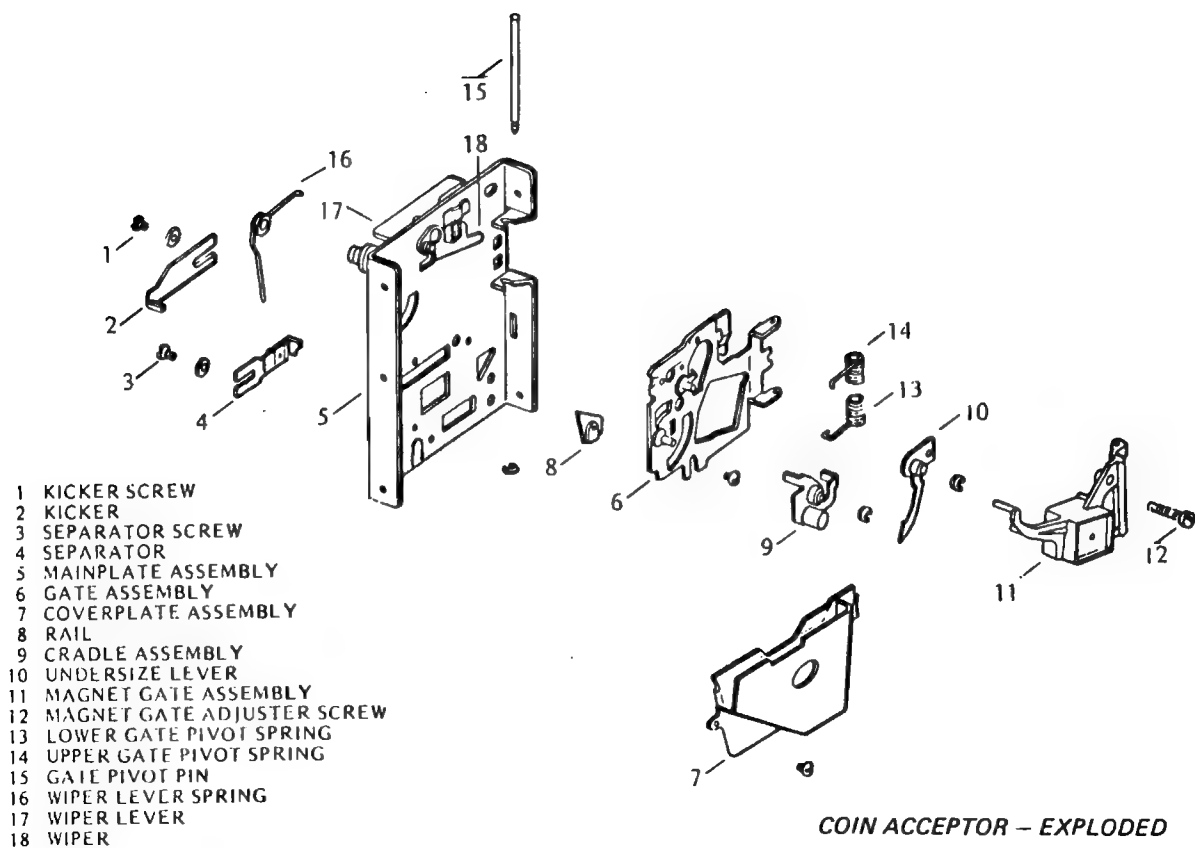
1. Set the acceptor with the front of the unit facing you in the test position.
2. Turn the magnet gate adjusting screw (2) out (counterclockwise) until none of the coins will fit through.
3. With a coin resting in the acceptor, turn the adjuster in (clockwise) until the coin barely passes through the magnet gate.
4. Test this adjustment using several other coins (both old and new) and, if any of them fail to pass the magnet gate, repeat Step 3 until all the coins are accepted.
5. Fix the magnet gate in this position with a drop of glue or lok-tite, if necessary.

c. Acceptor Maintenance

Depending on the environment in which the acceptor is used, periodic preventative maintenance should be performed. The mainplate (5) may be cleaned with any household cleaner. Thorough rinsing and drying are necessary to remove deposits and/or film. Remove all metal particles from the magnet by guiding the point of a screwdriver or similar tool along the edges of the magnet. You will notice that the particles will cling to the point of the tool. Remove the transfer cradle (9) and the undersize lever (10) and clean the bushings and the pivot pins. A pipe cleaner is an effective cleaning tool. Apply powdered graphite or pencil lead to the pivot pins and bushings and reassemble. Spray the entire unit lightly with WD-40, a silicone lubricant.

1-7. GENERAL MACHINE MAINTENANCE

Due to its solid state circuitry, your machine will require very little maintenance other than periodic cleaning, lubrication and T.V. monitor adjustment. The cabinet and plexiglass screen may be cleaned with any non-abrasive household cleaner. The coin acceptor and the rejector linkage should be sprayed lightly once every three months with WD-40 or similar silicone lubricant. The potentiometer shafts must never be lubricated in any way. The T.V. monitor is adjusted only when the CRT picture is distorted, or if the contrast or brightness appear to be out of adjustment.

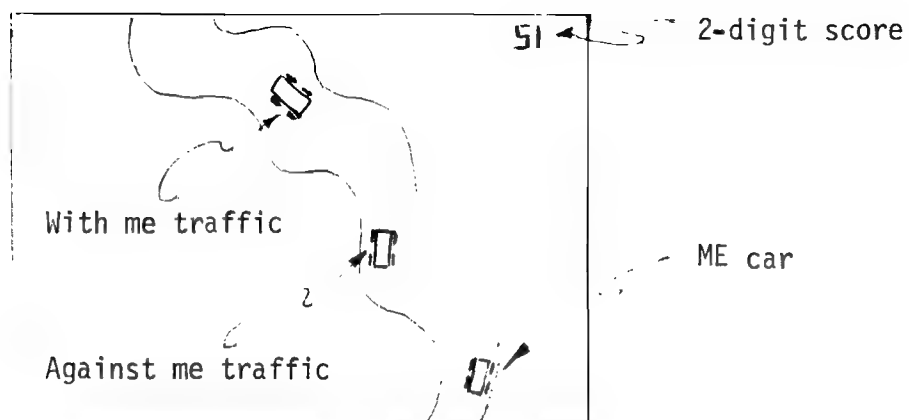


## Section 2 - Circuit Description

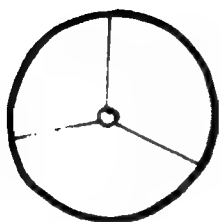
### HIGHWAY GAME

#### A. PLAY

##### 1. Display



##### 2. Controls



Steering Wheel



Coin Slot



Accelerator

The accelerator moves the road down. The steering wheel controls the ME car.

The ME car stays at the same relative vertical position in the lower half of the screen. Motion is the road moving down. If the car is off the road, only slow movement is allowed. On the road the ME car accelerates to a maximum speed.

The shape of the road is random. It can turn left or right to a maximum of 45 degrees. The digital memory for shaping attempts smooth curves. Because digital is quantized, there is some jaggedness at the edge of the road. The shape changes as a function of distance moved (not speed).

In the Attract Mode, the ME car is turned sharply to the right and moves in that direction as the road moves down. It does not stay on the road and when it reaches the right edge of the screen it disappears for a moment and shortly reappears at the left edge (still moving to the right).

In the play mode there are motor sounds from idle to full speed. OFF the road a graty beep-beep sound is added. Only relative slow speed is possible OFF the road. When hit by traffic a pulsing crash sound occurs while the ME car is pushed aside and motion stops.

Scoring is clocked off as distance travelled. A good score is possible only if you stay ON the road and avoid getting hit by traffic.

## B. CIRCUITS

1. Power (EE, FF-1)
2. Game Time Circuit (GG 1, 2, & 3)
3. Timing Circuits (DD 4, 5, 6, 7, & 8)
4. Video and Sync (DD 1, 2, 3)
5. Road Shaping (AA and BB 1-8)
6. Speed Pulse Sync Lock (BB5)
7. Analog Speed Circuits (BB 3 and 4)
8. Data Accumulator (BB 5 and 6)
9. Data IN Register (CC 5)
10. Memory Entry Control (1024 Bit S.R.) (CC 6-8)
11. Memory (1024 Bit S.R., Gate F1) (DD 6)
12. Memory Read Circuits (CC 5)
13. Road H Functions (EE 2-3)
14. Traffic Motion Functions (FF 7-8)
15. Traffic Car Building Circuit (EE 7-8)
16. ME Steering Circuits (EE 3-7)
17. ME Car Motion Circuits
18. OFF Road and Crash Circuits (CC 4-5)
19. Score Counters (GG 6-8)
20. Score Functions (FF 6)
21. Audio (BB 1 & 2)
22. Motor Sounds (BB 2 & 3)
23. Crash Sounds (BB 3 & 4)
24. Off Road Sounds (BB 2)

## 1. Power - EE, FF-1

Normally it is expected that +5 volts for the logic will be obtained from the TV set. It then comes in on the +5 volt terminal. In the event that we do not want +5 volts, we can use +10 volts unfiltered from the TV. That means a jumper is placed in a diode detail and +10 volts come in on one of the terminals (AC for 5 volts). The other alternatives provided for are AC center tap transformer or AC bridge rectified transformer.

+15 volts has its own rectifier and regulator (LM340T-15) section. Bridge and center tap alternatives are provided for. Another alternative for 15V regulation is to use a LM309 and associated network.

## 2. Game Time Circuits - GG 1,2, & 3

Game time starts when voltage is applied to 4.7K via input terminal. The coin counter is also connected at this point. The diode to +5 volts holds inductive spikes down.

Voltage must be at the input long enough for the 1 ufd cap to integrate up to transistor conduction. When this happens, FF of F9,6-8, 74132 hysteresis gate is set. The hysteresis gate also helps guard against spark false starts. The set of this FF is GAME TIME.



GT true releases 555 to pulse. The 555 pulses are counted. 8 counts is a game. The terminal count resets GAME FF via gate  $F8_3$ . A transistor is also connected to the reset gate to assure reset when power is applied or when there is an interruption in power.

If the EXTENDED GAME FF,  $F7_4$  gets set during the course of a game, a pulse is generated to restart the game counter from ZERO (via  $F8_6$ ). The last 1/8th of game time is sensed to generate a score flash functions ( $D8_6$ ).

### 3. Timing Circuits (DD 4-8)

Timing functions use 12.096 MHz crystal for simple countdown to H frequency. Interlace is not used in V. The end of the H countdown is at H sync. The V countdown goes to 128V which is decoded to V sync at DD 3. Countdown is continued to 8F for flash functions.

#### 4. Video and Sync DD1-3

Composite video is constructed to be compatible with Motorola and Ball Brothers T.V. monitors. Motorola TVs as used in prior Atari games have had internal blanking of H and V retrace and internal separation of synchronization from composite video. Ball Brothers monitors have neither of these and require separate H and V sync as well as a properly blanked video signal.

Composite video is constructed for Motorola monitors and a separate output is provided. Video without sync, but with blanking, is provided for the Ball Bros. monitor, 0-5 V.

A new video structuring method is used. Construction is for 3

levels of video: (1) Black

(2) Medium (medium white)

(3) White - this appears intensely white whether written on a black or medium background.

Two open collector outputs provide this video capability. These are from gates J9<sub>4</sub> and J9<sub>12</sub>. This is similar to gate A and B in the following circuit:

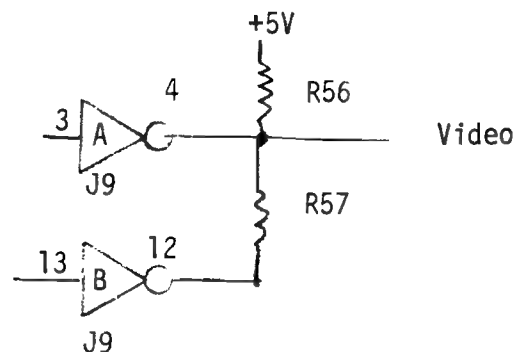


Figure g

Here video will be black if gate A is down (zero volts). Video will be medium if gate B is down (2.5V). Video will be white if gates A and B are both up. (5 volts).

Blanking is new to Atari games, but here it dominates. V blanking is constructed in latch F7 (DD 3) and horizontal blanking in latch P3 (DD 5). These are ORed to form composite NOT blanking in gate H7, 7402 (DD 3). Blanking forces gate K9<sub>6</sub> and K9<sub>11</sub> up. This makes the output of gate K9<sub>8</sub> go down forcing black and deleting all other signals. When blanking is OFF, background and black level are routed through negative OR gate N3<sub>8</sub> (DD 2). The resultant video switching is between ground and 2.5V (because gate J9<sub>12</sub> is down).

White signals are already OR when they input (+ true) to gate K9<sub>11</sub>. (ME car + score). These signals are down at K9<sub>4</sub> and J9<sub>13</sub> and force the output white.

The above provides video with blanking at levels satisfactory to Ball Brothers' video needs. Additional resistor matrixing inserts sync for Motorola. (R58, R60, and R59).

When sync is present the Ball Brothers output is already shorted to ground by blanking and thus there is no sync interference to the Ball Brothers' output. Without sync the Motorola output would swing from +5 volts to +2.5 volts with medium level at 3.75 volts. R60 adjusts the amount of sync that is added below blanking. 30% of the total swing is the value with given resistors.

## 5. Road Shaping

General principles: We desire to keep the shape of the road in digital memory. To do this we remember the top of the road in an 8-bit left/right counter C5 and B5 (AA 3-4). To change the road's shape we increment or decrement this counter. These changes are to the top of the TV display only. The second line down from the top is as the road was before a motion function made a new entry. Thus we have top of picture memory. A 1024-bit shift register is used to remember each incrementation or decrementation as it occurs. Thus a "stopped" road starts somewhere on the top and is apparently shaped as we look down. Sensible shaping necessitates a program. This program states that we will stay on the same slant for at least 8 lines. (Counter C6, BB 6). The program also states that when we change to the next slant we change only to the next angle. There are 8 different slants to the left and 8 to the right. For example, when we change from #4 to the left (for 8 lines), the next possibilities are no change (#4L, or #3L, or #2L). Any greater change would not be smooth in appearance. This sequence of angles comprises a curve.

The basis for a new entry to the top of the road is motion. Motion is defined by advance pulse. In this system we call these advance pulses "speed pulses" (SP). Distance travelled is determined by the number of these used. Speed pulses are generated in analog speed circuits. These are conditioned (BB 7-8) for synchronization and to limit the number to a maximum of 3 per field. The conditioned speed pulses are the input to the Road Shaping Circuit (A + F6<sub>8</sub>).

Specific Operation: Road direction and slant are stored in E7 (74193, BB 7). The direction is the most significant bit. For a right curve, the least significant bits show up unaltered at the outputs of exclusive gates E6<sub>3</sub>, E6<sub>11</sub>, and E6<sub>8</sub>, 1000 to 111). For left cruves, the direction bit changes, thus inverting the output of the exclusive gates. The result is again 000 to 111. The effect is that direction and magnitude signals are available. The magnitude will not wrap around from input (count inputs) because the borrow output (pin 13) is inverted and fed back to clear (pin 14). This means that after count has reached ZERO a countdown pulse will not be accepted because it is overridden by a reset (to ZERO). Conversely, the carry output (pin 12) is connected to the load input (pin 11). Since the inputs (pins 15, 1, 10, and 7) are pulled up, an attempt to wrap around after the counter is full reloads Full count and wrap around is not possible.

The number in the slant store defines slant by programming pulses in each 8 line interval. The 8 Speed pulse interval is counted by C6 (BB 6, 7493). The units that are represented by an incrementation or decrementation are one part in 256/ This is to the right or left. Only one can occur per line and since there are 256 lines, 45 degrees is the maximum slant the road can have.

Curves are made up off slanted sections that are changed by no more than one unit slant every 8 lines. A ZERO slant store means that no shift will be made. The number of increments or decrements that occur is the result of the gating program of gates D6<sub>8</sub>, D6<sub>11</sub>, and D6<sub>6</sub> (AA 5).

These gates are enabled by the 4's, 2's, and 1's bits of the slant store. The 4's bit permits 4 increment or decrement pulses to occur per 8 lines if it is ON. The 2's bit permits 2 pulses to occur per 8 lines, and the 1's bit permits only one pulse to occur per 8 lines. The pulse source for gating is the ORed (tied together) open collector output of C7, 74145, BCD to decimal decoder. The output of this system is at 7410, D5<sub>12</sub>, AA 5. From here it goes to increment the top of the picture, C5 and B5, AA 3 and 4, and to the data accumulator F5, BB 5. The count pulse to the slant store E7 forms the curves. No more than one count pulse can occur per 8 lines as limited by decoding of counter C6 at BB6. The forming of curve is a random program that at each 8 lines decides whether to make a change and if so whether the change be left or right. The direction of the next change is stored in C8<sub>9</sub>, 7474 (AA 7). If the road is to the FAR right and going right, FF C8<sub>9</sub> is forced left via PRESET input from gate B6<sub>8</sub>. Conversely, if the road is far left and going left, gates A5<sub>6</sub>, B8<sub>11</sub> reset FF C8<sub>9</sub> to force direction back to the right. This direction force is necessary to keep the road generally centered on the screen. Most of the time the direction FF is under the control of random programming via FF, C8<sub>12</sub> which determines direction (as discussed) and FF, C8<sub>5</sub> which determines whether or not to make a change (duration of curve). For RANDOM pulses we use RFX and RFD BB 2 and 3 which are functions of motor count counters. This is totally random with respect to the synchronous system because they count unprocessed speed pulses. Processed speed pulses can use only 3 per field and these must occur in the first half of the picture. While RFD is a divide by 2 of RFX, they are independent if read together at random times.

FF C8<sub>5</sub> controls the curve-making process. It decides the duration of a particular curve and whether there shall be a curve or not. There is no change of direction except when control FF C8<sub>5</sub> has just flipped up. (Clocking FF C8<sub>9</sub>).

The pin 2 input to FF C8<sub>5</sub> is a random number (generated in unprocessed speed pulses). This random number is interrogated when FF C8<sub>5</sub> is clocked via B8<sub>6</sub>. The time up (pin 5) is time when no change is permitted. During down time change of road slant is permitted. Thus the character of the road is determined by the ratio of these times. Function F (X) and F (Y) control this. F (X) is 8 times faster than F (Y). This means that change is permitted only half the time. This also means that a curve is maintained for seven-eighths of the time.

#### 6. Speed Pulse Sync Lock (BB 5)

The purpose of this circuit is to retime the random speed pulses. They enter the sync lock circuit at pin 4 of F6<sub>6</sub>. The synchronized speed pulses are restricted to the top half of the pix by  $\overline{128V}$  at D5<sub>5</sub>. XPP are pulses 4V long generated in forming vertical sync (DD 3). There are 4 of these in the upper half of the pix. They are routed through inverter D1<sub>2</sub> to gate D5<sub>3</sub> and the output speed pulses occur at pin 8 of F6. The 7474 is the random speed pulse detector. If a random speed pulse is detected, the next synchronized pulse is permitted to pass in full. The set input is the detector. It cannot set the FF if the random pulse comes up in the middle of a timed pulse, however any random pulse that occurs between latch gates the FF and the next timed pulse through in full. Three pulses per field is maximum speed as far as the digital circuits are concerned. After 3 pulses have been

detected, the reset input to the FF H6<sub>9</sub> is held down (from pin 8, gate A4 - CC 7).

#### 7. Analog Speed Circuit - BB 3 & 4

Timer 555 (BB 3) pin 3 output is of random speed pulses (negative true). The pulses duration must be less than 4V so that they can be properly retimed by the digital circuits. R22 and C18 determine this time. The rate at which the pulses occur is determined by the collector current made available by Q4. Since countdown of speed pulse generates motor and crash sounds, the 555 must be operating even when motion is stopped. The minimum current supplied by Q4 is determined by resistor divider R47 (47K), R42 (1.2 meg) and R43, emitter resistor. The combination places a voltage current to the 555 that is independent of transistor beta. Diodes CR7 and CR8 are connected to compensate each other for temperature variation. To get idle sounds without road motion, it is necessary to detect when the speed pulse rate is below a certain threshold. Devices N8<sub>5</sub>, K9, H9, and N8<sub>3</sub> are digital rate detectors to do this. It had been determined that good idle sounds occur when the spacing between unprocessed speed pulses is more than 8 ms. This is the threshold that the digital rate detector is set to. FF N8<sub>5</sub> and N8<sub>3</sub> are reset to ZERO by  $\overline{V \text{ SYNC}}$ . After that they can count to 3, but no further. If at the next reset time they have counted to 3D, FF sees it and holds the G0 level. On the other hand if the count of 3 is not reached, D FF H9 sees this too. The generated G0 signal controls the input to the digital S.P. Sync lock at BB 8. G0 signals are also overridden during crash by the set input to DFF.



For speed in excess of idle, the voltage of R47/R42 divider is forced lower. The basic manipulation of this voltage is to the charge on C17 220 mfd BB4. If this charge is greater than the divider voltage, we have idle. Q1 is the crash transistor. It is connected to +15V in order to pull the charge up as fast as possible. When a crash occurs, 7406, B9<sub>8</sub>, turns Q1 ON and the charge rate is limited only by R39. C16 10 mfd holds the crash sound ON for a second or so. Q2 is the OFF-the-road speed limit transistor. It is operated by 7406, B9<sub>6</sub>. When the transistor is turned ON it limits the low voltage on C17 to a value established by the ratio of R32 and R30. Diode CR17 prevents this circuit from swamping the crash input. When neither crash nor OFF road charge is being supplied to C17, the idling voltage of C17 is kept near the threshold of change by divider R37 1K and R36 10K, BB 5. When gas is applied, C17 discharges through R33, 33K. This resistor determines the acceleration rate. When foot is removed from gas pedal, C17 charges up through diode CR3 and the Z of the divider. This charge is relatively faster to simulate some application of brakes without actually having separate brake control.

Not Game Time ( $\overline{GT}$ ) gives override road acceleration via R27 and gate B9<sub>10</sub>.

#### 8. Data Accumulator BB5&6

8 bit shift register F5 is used to store the events in the road shaping program (see #5). The storage is entered serially to form a data stream for updating the 1024 bit road memory SR E1. The data is organized in 2 bit groups, one group for each speed pulse (maximum of 3 per field).

Each SP gives two advances to S.R. via F1, 7402. The first advance enters direction L/R gate E4, BB6. The second enters enable bit. That is direction is irrelevant unless it is enabled. As many conditional S.P. pulses as occur enter data into the data accumulator.

#### 9. Data in Register CC5

Data is transferred broadside from data accumulator (8 above) at ME-CAR time (MCW gate A4 ). This is after all speed data has been accumulated in this field. The data IN register is now ready to shift information into the road memory. (1024 bit S.R.) The shift is in the opposite direction to that in which it was entered in the data accumulator. That is, Enable comes out before direction. The last entered data comes out first. The combination of data accumulator and data IN register is equivalent to an 8-bit shift-left/shift-right register.

When data is needed for entry into road memory (1024 bit S.R.) gate H5 CC5 shifts it out under control of (10) Entry Control.

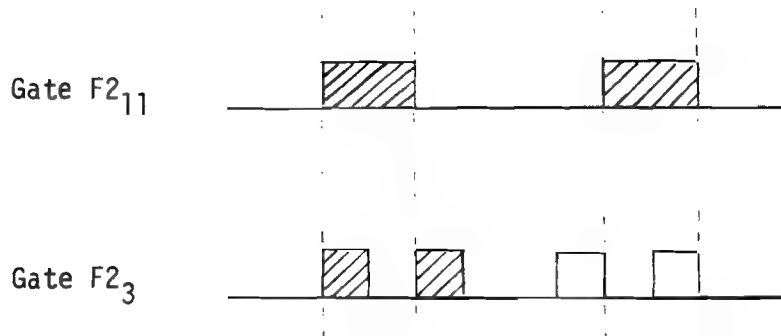
#### 10. Memory Entry Control (1024 bit S.R.)

When the road is not moving the contents of memory (1024 S.R.) is rotating synchronously with line count. There are 256 lines in a field so the memory rotates 4 bits per line. Two bits per line is all the information that is used.

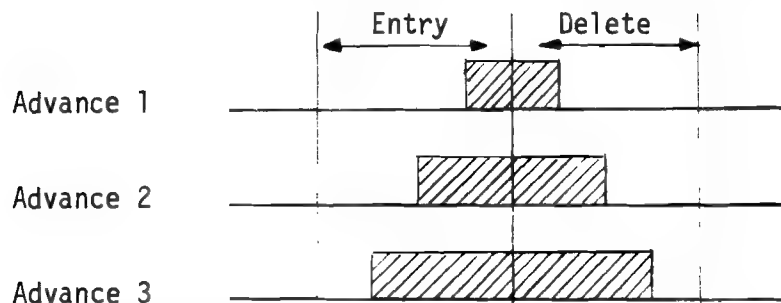
The time we must update memory is at the top of the picture. The first entry (for first line) is top of picture memory. Subsequent information from memory is increment/decrement information. If we want to advance one line (motion), we must capture the last bits in the memory chain and replace them with new data. Then to actually do the motion we must delete one line of memory advance. This procedure places the incremented data that was for the first line into the second line position and places new data into the first line position. For the purpose of entry, this means that the last line must be anticipated for the purpose of changing it prior to entering the new data, then we delay by deleting advances. Similarly, if the advance is to be for 2 or 3 lines, the amount of anticipation must be increased accordingly.

The anticipation circuits are counter J1, CC7 and 8, which counts the speed pulses processed in speed pulse sync lock. This counter is set to 11 in the 4th period following the end of V sync to prepare the counter to capture the next speed pulses. The count is 11 to 00 to 01 to 10. 10 is the third count. This is decoded in gate A4<sub>8</sub>, CC7 and routed to prevent further use of speed pulse by road shaping circuits. The period that is used for update is 4 lines during V sync and the 4 lines afterward. Since V sync is 4 lines long, this defines the beginning period. FF P3, 279 CC8 uses V sync and 4V to generate a pulse that bridges this time (before and after). Only 3 lines before and 3 lines after are actually used in updating. The last line (after) is used to reset the S.P. counter for use in the next entry.

Bridging functions are generated in exclusive gates below, giving the following waveforms:



When these functions are compared with the content of the counters, gate  $F2_8$  and gate  $F2_6$ , the 3 use output forms are:



Left of center is for entry, right of center for count delete. Entry is decoded at gate  $E2_6$  for switching entry (pin 3 of memory gate  $E1$ ). Delete count is done from gate  $F4_8$  which inputs to gate  $E2_8$  for deleting advance counts.

## 11. Memory (1024 Bit Shift Register, Gate F1)

A 1M7733 (Intersil) or a 2533V shift register can be used. With the 2533C, -12 volts is required at pin 2.

Data input terminal is pin 5. Recirculation is pins 1 and 7. Most descriptions are being done in terms of input and output requirements.

## 12. Memory Read Circuits - CC 5

Top of the road memory is C5 and B5, AA 3 up/down counters. The road write counters are C4 and B4, CC 4. At V sync time (top of picture) the contents of top of road memory are transferred to road write counters. This is a broadside load. Commencing with line #2, the road write counters are incremented or decremented with the contents of road memory (1024 bit S.R.). The road memory is only 2 bits for each line. The first of these bits is direction. The next is enable. Direction is read by DFF E4. This FF is connected to gates D4<sub>6</sub> and D4<sub>3</sub>. If the direction is right, gate D4<sub>3</sub> is enabled to permit road write counter to be incremented. Conversely, if left, the decrementing gate is enabled. The instruction is executed only if the next bit is an enable bit, otherwise for that line there is no change. The process continues through all 256 lines in the picture. Thus, the road write counter traces out the shape of the road. The gated functions are designed so that "trace out" is the left edge of the road. Comparators B3 and C3 compare the contents of road write with TV horizontal functions. The output of these comparators is a very short pulse (2H) which is used to trigger the road H function counter, M8.

This pulse is improved by clamping to 5V and using 15V for Vcc source. Additional delay for 2H functions avoids problems of missing pulses that can occur because of non-synchronous counters.

### 13. Road H Functions EE 2-3

M7 and N7 are the road horizontal counters. It is a 6 bit counter (3 bits in each of 2 7493s). M8 JK F.F. is count control. The road write compare triggers the reset input of the control FF and 6 bits are counted through before the clock input senses the end of count and turns OFF the H count pulses (gate L8<sub>6</sub>). The road dimension is a whole 64H function, which is one-fifth of the TV horizontal dimension. The output of the control FF is the road. To generate a dotted center line in the road, the rising edge of 64H is sensed by digital mono P3 74279 CC 2, which because of fast reset (1H) generates a narrow line. This line is chopped by memory shift pulses. The route is gate B1<sub>8</sub> CC6 to gate D2 CC6 (AFT) to gate P3 and divider N3 CC8. Memory shift pulses must be used if the chop in the road is to move with the road.

### 14. Traffic Motion Functions FF 7-8

The memory shift pulses counted down by one FF K\$<sub>12</sub> (HH8) are fixed with respect to the road. That is, if the road moves so does this function. To generate motion for traffic, we want to add to or subtract from this function for motion up or motion down. The basic memory shift pulses are divided by 2 (FF K4<sub>12</sub> HH8). That means if we delete one count per field we create motion up at a rate equivalent to the same motion of the road created by acceleration. Maximum acceleration is at the rate of 3 pulses deleted per field. Therefore, the traffic speed created by

2 pulse deletions is  $2/3$  of maximum as desired. Gate  $L3_3$  ANDS  $2V$  with  $V$  sync to generate a pulse of the proper width to capture and delete one counted down motion pulse. At gate  $L3_6$  this is ANDED with divided down shift pulses to do that. Six bit counter  $K3$  and  $K4$  work from motion processed pulses to form  $V$  function for downward moving (opposing) traffic car shaping. The count pulses for the upward moving cars need to get one pulse ADDED for proper 2 bit motion. To do this we use the  $V$  sync AND  $2V$  period in the same manner as the delete function, (via gate  $L3_{11}$  and gate  $L3_8$ ), but we chop it with the horizontal function dots  $K4_{12}$ . Thus, in the delete period we add 2 faster pulses, that is  $-1+2 = +1$ , as desired.

#### 15. Traffic Car Building Circuit EE 7-8

Cars are built from vertical motion function and horizontal road function. The major vertical functions that define the length of the car are decoded at gate  $L4_8$  GG7 7420 for upward moving traffic. For the downward traffic, the same thing is done at gate  $L4_6$  FF7 7420.  $32HR$  and  $16HR$  are compared in exclusive gate  $M6_{11}$  to give the major horizontal limits for both cars. Traffic downward is ORed with traffic upward at pins 5 and 4 of gate  $N6$  GG6. Downward traffic is gated by  $FF$   $H6$  GG6 and  $2F$  in order to thin downward traffic. There is traffic in every field moving upward to ME car, but downward, to make passing feasible, traffic appears only in every other field. To do this the motion function for the downward car is divided after its formation (inverter  $L5$  pin 4). The divide function is up for one field and down for the next. The switch occurs where the car is so we interrogate every other field during  $V$  sync time with  $2F$  (pin 3 of DFF  $H6$ ). This enables the

down car to be present only every other field. That is, it disappears travelling one whole V dimension in limbo. Cars are ORed in gate  $N4_6$ . The up car is assembled in OR gate  $N4_3$  where wheels and body come together. Similarly OR gate  $N4_{11}$  is used for the down traffic.

The difficulty of the game can be increased by a DIP switch at  $L4_{12}$  which doubles traffic in the same lane, and/or a DIP switch at  $H6_5$  which doubles the traffic in the opposing direction.

#### 16. ME Steering Circuits EE 3-7

The whole purpose of steering input is to enter a number into direction/magnitude counter J8 FF6. This direction magnitude counter works the same as the one in section 5. That is, count below zero or above 15 is inhibited by use of borrow and carry pulses fed back to either reset or load at these limits. Between these limits steering input changes the count in regular steps. Direction is recorded with the most significant bit. The 3 lesser significant bits are routed through exclusive gates  $K8_1$ , 4, and 8. Here they are inverted if the most significant bit is present. The resultant output counts upward whether we count down or



up (magnitude). If the output bits are zero, the ME car goes straight without steering correction. If there is a count present the ME car continues to turn as long as the wheel is not touched. That is it works just like a real car. The steering inputs are pulses to move the steering storage count up or down. The optically coded input gives quadrature pulse to hysteresis gate  $F9_3$  and  $F9_{11}$  (74132). Hysteresis gates must be used here otherwise slow transisions generate multiple pulses. FF H9 is the direction detection and storage device. It selects whether we will gate count pulse to count up or down (gates  $H7_{10}$  &  $H7_{13}$  ) FF7. FF M7 further counts down the steering pulse to give somewhat slower response in steering than happens, if we gate the quadrature pulse of the Atari designed encoder.

#### 17. ME Car Motion Circuits

The ME car motion circuit defines motion left or right. It is a synchronous counter with synchronous load capability J7 and K7 . The count is structured to be identical with the TV horizontal countdown, except we start to count with 1H to free the last FF in the second 74161 for the purpose of detecting the beginning of the next count cycle. Since we are also dividing by 3 in L6 74107 BB2 to detect the beginning cycle we must AND with begin count here. Gate K6 BB2 does this and supplies the load signal. The load signal will exist for only one count pulse since the next output has reset the last (detector) FF. This detector FF has made it possible for load to enter either counts ahead or counts behind without lockup. We want to give horizontal motion that is consistent with the angles of the road as it comes down. The maximum angle of the road is 45 degrees (almost).

When the maximum angle is true the road is incremented or decremented one 256th of the screen per line (almost). When the road is coming down at maximum speed the horizontal motion of the ME car must be able to match this. One 256th unit is equal to one (2 bit) unit in the horizontal motion counter. The motion by this unit is obtained by:

1	0000	Load Time
0	0001	Next count - no motion
0	0000	Next count - motion right
0	0010	Next count - motion left

Bits manipulated is seen to be only the least significant two and the detect bit. If input to gate J7 pin 3 (L.S.) is 1, the signal at 4 (2's significance) is forced to be ZERO. This is the condition for no motion. If on the other hand the gate J7 pin 3 input is ZERO, then either 0000 or 0010 is loaded depending on the polarity of the direction input to pin 6 of H7 7402 BB4. For the moment ignore exclusive gate K8 BB4 and assume that the direction signal passes through from pin 2 to pin3 with inversion only. We see that the source of the motion pulses is a programmer of the same kind that is used to form the road. Here the 74193 gate J8 (FF6) - direction and rate memory) is similar to the 74193 gate E7 (direction and slant). This makes possible motion rates for the ME car that matches any slant in the road. The source of the pulses that implement ME car motion is the same as the road motion pulses. Via gate A4 pin 5 to pin 6 (EE7) and pulse programmer counter N9, decode SP and pulse routing gates  $L8_3, L8_{11}$  &  $L8_8$ . Thus no matter what rate the road is moving there is a ME car motion number that will match it.

It should be noted that actually the road can be incremented only 7 out of 8 pulses since there are only 7 outputs used in the M9 (EE6) 74145. Using an additional bit in association with the most significant bit for ME car motion gives a small added increment of motion that permits that car to get back on the road against a 45 degree angle. The Motion circuits for the ME car are incremented at speed pulse time (one line only). The time from the middle of the picture to end is available for other manipulation of the motion counter and it is used to bend the car in the direction of its motion. We want the top to wag in the direction of motion (like a car) rather than to have the bottom wag opposite to the direction of motion (like a motor boat). To do this we count rapidly in the direction of motion before the ME car window, then during the ME car window we count back. Net motion is ZERO but we have bent (or wagged) the ME car. The speeded up count is gated into ME car motion at gate L7 FF5 (2V & S.R.) and into the slant program at gate A4<sub>3</sub> EE7 (IV). The direction of the first half of this count is forward. In the later half we count backward. Exclusive gate K8 FF4 uses the ME car window to make this switch. Gate K6 BB5 is operational only during V Sync and is used to push the ME car aside in a crash.

#### 18. OFF Road and Crash Circuits CC4-5

OFF road coincidence involves feedback to the analog speed control already discussed in section 7. The coincidence of OFF the road are digital circuits. The problem of interface is that digital coincidence is a very short pulse. Too short to use directly as feedback to analog control. We solve the problem with a digital mono (gate F7 74279 (GG5)). This FF is set with the short coincidence pulses from gate F6 (GG5) pin 11. The reset is at a time just prior to the next ME car V window (decoded in gate A6<sub>12</sub> ).

This means that coincidence pulses are at least 12 ms long. The same set and reset philosophy is used for collision of ME car with traffic. Decoded in gate F6<sub>3</sub> and setting FF F7, 74279. The reason we stretch this pulse is so that any collision will have a level available during V sync so that at this time we can gate a limited number of ME car motion pulses to have the car pushed aside by the collision. V sync permits 4 motion pulses. The crash pulse is stretched at the collector of B9<sub>8</sub> (BB 5) by 10 mfd capacitor C16 to give a reasonable crash time.

#### 19. Score Counters GG 6-8

Score is simply counting of speed pulses that are actually used to advance the road. The counting chain is C6 93 ( 1 bit), A8 93 (4 bits), A7 93 (4 bits), N2 90 ( 4 bits), and L2 93 ( 4 bits). The last two 4-bit counters are decoded to generate score. We count from 00 to 99 legitimately. If both counters were 7490s, count would wrap around to ZERO in the event of very high scores, but because we use a 7493 in the most significant counter and a 7448 to decode it, a different symbol appears at count 10 instead of wrap around.

#### 20. Score Functions

74157 gate M2 (HH 6) is a multiplexer (4 pole, 2 position switch equivalent) for time sharing the 7448 seven segment coder. 9312 multiplexer gates the segment to the required TV times, L1 handles the horizontally written segment, and N1 handles the vertically written segment. Score and road are ORed in gate K1, 7420 (HH 5). Score and ME car video are present at pin K9<sub>13</sub>.

## 21. Audio BB 2 & 3

A LM380 is used for audio output. Mixing off OFF road, motor, and crash sounds occurs at top of the volume control pot.

## 22. Motor Sounds BB 2 & 3

Motor sounds are generated from countdown of the non-processed speed pulses. Counter N9 and C9 give a divide by 4. This is mixed with divide by 3 the divide by 6 derived from counter C9 (7492). The mixing resistor mixes approximately equal components of these frequencies. They are integrated by .1  $\mu$ f C28. The R24 330 ohm permits a little high frequency to sneak through giving some sharp picking in the sound.

## 23. Crash Sounds BB 3 & 4

To generate the crash sounds the output of Q1 is routed 3 ways:

1. Via CR4 and R39 (1.5K) to pull up the charge of C17. This gives it a proper charge for a slow restart after the crash.
2. Via R40 and CR6. This speeds up the 555 speed pulse generator to give a screechy crash sound.
3. Via R41, 10K, to operate Q3 and gate B9<sub>2</sub>, 7406, to remove motor sound integrater C28 from circuit during crash. This changes the sound to make it very raspy. Q3 also has a connection to set H8 D.F.F. This forces motion to stop during the crash.

We improve crash sounds by pulsing the sound integrator on and off via B9 pin 4. The pulse rate is approximately four per second.

Crash sounds generated this way tend to have overpowering volume compared to normal motor sounds. To limit this volume, R18 and diode CR2 hold volume down during a crash.

#### 24. Off Road Sounds BB 2

These sounds are gated in D8, 7420. They are enabled only if the car is moving and OFF the road. Functions 8F and 4V give a beep-beep effect.

### C. TESTING

Game set up requires:

1. Steering assembly using EL740419-3 steering board.
2. Coin switch assembly.
3. Stancore F40-X transformer for 15 volts - optional 16.5 volts center tap transformer for 5 volts.
4. XM501 Motorola TV chassis or TTL 23C/AC Ball Bros. TV chassis.

PCB is designed to get 5 volts either from Motorola TV chassis or from an ON board power supply.

A Tektronics 465 oscilloscope or equivalent is a necessary test instrument for PCB testing.

This circuit explanation was given in the logical sequence for testing.

In other words, at a given point all preceding circuits must be functioning to allow subsequent tests to be meaningful.





### 3. CUSTOMER SERVICE INFORMATION

#### 3-1. TEST EQUIPMENT

In order to test any Atari PCB, some items such as the logic probe are absolutely essential. Others are desirable and will make the test procedure easier but are not absolutely essential. Some of these instruments are available from the Atari Customer Service Department and these are: the Kurz-Kasch 520 Logic Probe, the Atari Video Probe and the Hewlett-Packard 10529A Logic Comparator. Other instruments that are very useful are the HP 10526T Logic Pulser and the Tektronix 465 Oscilloscope. These items are available through your local electronics supply house.

#### 3-2. REQUIRED MINIMUM EQUIPMENT

The following items are absolutely essential to perform the test procedures presented in this manual:

- a. Logic Probe: The logic probe is an instrument designed for checking the outputs of integrated circuits. The Kurz-Kasch Logic Probe, Model No. LP-520, which is available through the Atari Customer Service Department or most large electronics supply houses, is recommended. This logic probe indicates if a signal is a logic high, logic low, or changing from one state to another. Consult the operating instructions included with the probe for further details about its operation.
- b. Video Probe: The video probe is a very simple but extremely useful device and consists of two test clips, a length of rubber-coated, test-lead wire, and a 4.7K,  $\frac{1}{4}$  watt carbon resistor. Video probes may be obtained from the Atari Customer Service Department or, if necessary, they can be assembled from standard components available at all electronics supply houses.

### 3-3. OPTIONAL EQUIPMENT

It is possible to find 90% of the possible PCB computer malfunctions without the following items. However, if a complete set of troubleshooting equipment is desired, Atari recommends:

a. Hewlett-Packard 10529A Logic Comparator

The Hewlett-Packard 10529A Logic Comparator is used to verify correct IC operation. This device simply clips onto in-circuit ICs and instantly displays any logic state difference between the in-circuit test IC and the reference IC in the comparator. Logic differences for each pin of a 14 or 16 dual in -line package are indicated by a lamp on the comparator. If the logic comparator is purchased from the Atari Customer Service Department, it is shipped with 20 preprogrammed reference PCBs. If the device is purchased elsewhere, these PCBs must be specially programmed.

b. Hewlett-Packard 10526T Logic Pulser

The Hewlett-Packard 10526T Logic Pulser is used to stimulate in-circuit ICs so that they are driven to their opposite states. This device is available from the Atari Customer Service Department or can be obtained from most large electronics supply houses.

c. Tektronix 465 Oscilloscope

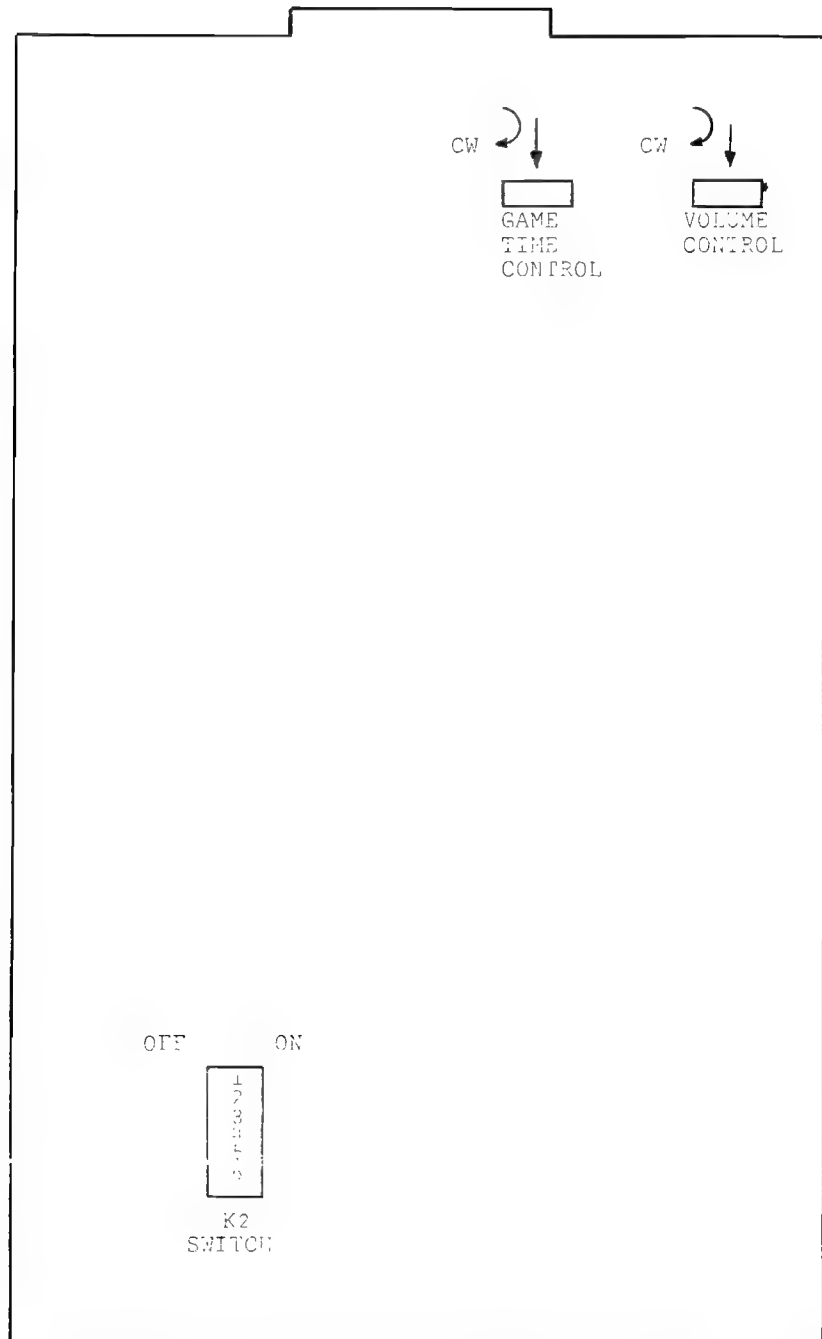
The Tektronix 465 Oscilloscope is used for viewing various wave forms and should be ordered from Tektronix. Consult the manufacturer's operating instructions for details on oscilloscope operation.

## LOGIC TYPE & FUNCTION

<u>TYPE</u>	<u>FUNCTION</u>
7400	QUAD 2-INPUT NAND GATE
7402	QUAD 2-INPUT NOR GATE
7404	HEX INVERTER
74S04	HEX INVERTER
7408	QUAD 2-INPUT AND GATE
7410	TRIPLE 3-INPUT NAND GATE
7413	DUAL NAND SCHMITT TRIGGER
7420	DUAL 4-INPUT NAND GATE
7425	DUAL 4-INPUT NOR WITH STROBE
7427	TRIPLE 3-INPUT NOR GATE
7430	SINGLE 8-INPUT NAND GATE
7448	BCD TO 7-SEGMENT DECODER
7450	DUAL AND/OR GATE (INVERTER/EXPANDER)
7474	DUAL D FLIP FLOP
7483	4-BIT FULL ADDER
7486	QUAD EXCLUSIVE OR GATE
7490	DECADE COUNTER
7492	DIVIDE-BY-12 COUNTER
7493	4-BIT BINARY COUNTER
74107	DUAL JK M/S FLIP FLOP
74153	DUAL 4-BIT MULTIPLEXER
74157	QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER
74165	PARALLEL-LOAD 8-BIT SHIFT REGISTER
74192	SYNCHRONOUS DECADE UP/DOWN COUNTER

74193	SYNCHRONOUS BINARY UP/DOWN COUNTER
LM380	AMPLIFIER
NE555	TIMER
NE566	FUNCTION GENERATOR
747	DUAL OPERATIONAL AMPLIFIER
RC4136D	QUAD OPERATIONAL AMPLIFIER
MFC6040	VOLTAGE CONTROLLED OPERATIONAL AMPLIFIER
8098	HYBRID
8103	HYBRID
8099	HYBRID
9311	ONE-OF-SIXTEEN DECODER/DEMULTIPLEXER
9312	8-INPUT MULTIPLEXER
9314	QUAD LATCH
9316	4-BIT BINARY COUNTER
9321	DUAL ONE-OF-FOUR DECODER
9602	DUAL MONOSTABLE MULTIVIBRATOR
74186	ROM

HYWAY OPERATOR INSTRUCTIONS  
003634 REV. A



- \*1. GAME TIME CONTROL. TURNING THIS CONTROL CLOCKWISE INCREASES GAME TIME.
- \*2. VOLUME CONTROL. TURNING THIS CONTROL CLOCKWISE INCREASES THE VOLUME.
3. PLAY OPTIONS: (CAUTION - FOR DIFFICULT GAME ONLY)
  - A. K2 SW 1 OFF DOUBLES OPPOSING TRAFFIC.
  - B. K2 SW 2 OFF DOUBLES WITH ME TRAFFIC.
4. EXTENDED PLAY SCORE LEVEL: (SUM OF NUMBERS SETS THE SCORE LEVEL AT WHICH GAME TIMER IS RESTARTED FOR EXTENDED PLAY).
  - A. K2 SW 3 ON GIVES 10 POINTS.
  - B. K2 SW 4 ON GIVES 20 POINTS.
  - C. K2 SW 5 ON GIVES 30 POINTS.
  - D. K2 SW 6 ON GIVES 40 POINTS.

NOTE: EXTENDED PLAY SCORE SWITCHES SHOULD ALL BE ON TO AVOID GIVING EXTENDED PLAY.

\*DIRECTION OF ROTATION IS DEFINED WHEN LOOKING IN DIRECTION OF ARROWS.





ASSEMBLY TITLE / ARCADE DRIVER - TOP ASSY

P/L 003209

PARTS LIST SPECIFICATION

Page 1 of 1

Drawn Regan Cheng

Checked M2. 3/12/75

Proj. Eng. REGAN CHENG

Mech. Eng. J. J. J.

Elec. Eng.

REV.  
A

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A		3-11-75	EC				

Item	Part Number	Qty.	DESCRIPTION
1	A003190	1	Cabinet Assembly
2	A003150	1	Seat Assembly
3	003210	1	Angle, Connector
4	75-5520N	10	Bolt, Carriage, 1/4 - 20 x 1 1/4 Lg.
5	75-015S	10	Washer, Flat, Steel, Reg. Pattern, # 1/4
6	75-045S	10	Washer, Lock, Split, # 1/4
7	75-915S	4	Nut, Hex, # 1/4-20
8	75-935S	6	Wingnut, Steel, 1/4-20







## ASSEMBLY TITLE

DASHBOARD ASSEMBLY

P/L 003134

## PARTS LIST SPECIFICATION

Page 1 of 1

Drawn REGAN CHENG

Checked M.2.

Mech. Eng. V. J. J.

Proj. Eng. V. J. J.

Elec. Eng.

REV.

C

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A	Rev per	3-11-75	R. N.				
B	Rev per ECN 1251	3-19-75	R. N.				
C	Rev per ECN 1303	4-7-75	R. N.				

Item	Part Number	Qty.	DESCRIPTION
1	003132-01	1	Panel, Dashboard
2	A000598	1	Steering Wheel Assembly, (12" Dia. Wheel)
3	003137	1	Panel, Back-up
4			
5	000567	1	Bow Washer
6	62-008	1	Switch, Licon #01-700158 (Omit on Highway Game)
7	001856	1	Bezel, Start Switch (Omit on Highway Game)
8	72-1112S	6	Screw, Mach, Pan Hd., Phil. #10-24 x 3/4 Lg.
9	A000607	1	P.C. Board Assy, Steering
10	73-1206	2	Screw, Machine, Phil hd., #2 x 3/8 Lg.
11	A003470-01	Ref.	Main Harness Assy, Highway



ASSEMBLY TITLE

FOOT PEDAL & BOX ASS'Y

P/L 003567

PARTS LIST SPECIFICATION

Page 1 of 1

Drawn H.WOLFF

Checked

Mech. Eng.

Proj. Eng. H.WOLFF

Elec. Eng.

REV.

A

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.

Item	Part Number	Qty.	DESCRIPTION
REF.	A003567		FOOT PEDAL & BOX ASSEMBLY
1	A001631	1	BOX, ASS'Y
2	75-1532S	3	SCREW, MACH: PHIL. PAN hd #1/4-20 x 2"lg.
3	75-915S	3	NUT, HEX 1/4 - 20
4	75-015S	6	WASHER, FLAT, 1/4"
5	75-2412S	2	SCREW, MACH, RD. HD. PHIL. #4/40 x 3/4 lg.
6	75-914	2	NUT, HEX #4/40
7	75-014S	2	WASHER, FLAT, #1/4"
8	75-054	2	WASHER, LOCK #4
9	65-071C	1	SWLTCH, CHERRY #E51-60B
10	-----	1	ACTUATOR WIRE PROVIDED WITH SWITCH
11	72-6810	2	SHEET METAL SCREW #8x 5/8 lg.
12	002191	1	BRACKET, SWITCH
13	A003470-2	1	HARNESS, FOOT PEDAL
14	A003511	1	SINGLE FOOT PEDAL ASSEMBLY; metal
15	75-918S	4	NUT, HEX #8-32
16	75-018S	4	WASHER, FLAT REG. PATTERN #8
17	75-048	4	WASHER, SPLIT-LOCK, #8



ASSEMBLY TITLE / ELECTRONIC TRAY ASSEMBLY

P/L 003340

## PARTS LIST SPECIFICATION

Page 1 of 1

Drawn Regan Cheng

Checked M. Z. 4/18/75

Mech. Eng. B. H. A.

Proj. Eng. Regan Cheng

Elec. Eng.

REV.

A

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A		4/18/75	K. J. S.				

Item	Part Number	Qty.	DESCRIPTION
1	003339	1	Electronics Tray
2	000622	1	Cover, Transformer
3	000871	1	Label
4	001551	1	Transformer
5	79-3201	2	Fuse Holder
6	46-20110	1	Fuse, 1 Amp, Slo Blo
7	90-3001	1	Filter, Power Line
8	54-401	1	Power Cord, 8'
9	72-6610	13	Screw, S.M., Pan Hd., Phil., #6 x 5/8" Lg
10	A001920	1	Harness, Voltage Selector
11	*A001921-01	A/R	Shorting Block, 95V
12	*A001921-02	A/R	Shorting Block, 110V
13	*A001921-03	A/R	Shorting Block, 220V High
14	*A001921-04	A/R	Shorting Block, 220V Low

\*Install Shorting Block per voltage requirements.



ASSEMBLY TITLE / P.C. BOARD ASSEMBLY - HYWAY P/L 003211

PARTS LIST SPECIFICATION Page 1 of 2

Drawn			
Checked <i>MJ. 3/26/75</i>	Mech. Eng.		
Proj. Eng.	Elec. Eng <i>HVS</i>		REV. <i>E</i>

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A	Rev. on	3/26/75	<i>HVS</i>				
E	REV PER ECN 1299	4/4/75	<i>HVS</i>				

Item	Part Number	Qty.	DESCRIPTION
1	37-7400	13	Integrated Circuit, 7400
2	37-7402	4	" " 7402
3	37-7404	11	" " 7404
4	37-7405	3	" " 7405
5	37-7406	1	" " 7406
6	37-7408	1	" " 7408
7	37-7410	7	" " 7410
8	37-7420	8	" " 7420
9	37-7427	2	" " 7427
10	37-7430	1	" " 7430
11	37-7448	1	" " 7448
12	37-7474	5	" " 7474
13	37-7486	7	" " 7486
14	37-7490	1	" " 7490
15	37-7492	1	" " 7492
16	37-7493	17	" " 7493
17	37-74107	4	" " 74107
18	37-74132	1	" " 74132
19	37-74145	2	" " 74145
20	37-9322	1	" " 9322
21	37-9316	2	" " 9316
22	37-74164	1	" " 74164
23	37-74165	1	" " 74165
24	37-74193	6	" " 74193
25	37-74279	2	" " 74279
26	37-9312	2	" " 9312
27	37-2533V	1	" " 2533V
28	37-555	2	" " 555
29	37-LM380	1	" " LM380
30	37-LM340T-15	1	" " LM340T-15
31	10-5270	1	Resistor, Carbon, $\frac{1}{4}$ Watt, 5%, 27 ohm
32	10-5100	1	" " " " 10 ohm
33	10-5181	1	" " " " 180 ohm
34	10-5561	1	" " " " 560 ohm
35	10-5331	5	" " $\frac{1}{4}$ Watt " 330 ohm
36	11-5391	1	" " $\frac{1}{2}$ Watt " 390 ohm
37	10-5471	6	" " $\frac{1}{4}$ Watt " 470 ohm
38	10-5153	1	" " " " 15K ohm
39	10-5223	1	" " " " 22K ohm
40	10-5102	1	" " " " 1K ohm

## PARTS LIST SPECIFICATION

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Item	Part Number	Qty.	DESCRIPTION
41	10-5152	2	Resistor, Carbon, $\frac{1}{4}$ Watt, 5%, 1.5K ohm
42	10-5222	2	" " " " 2.2K ohm
43	10-5272	21	" " " " 2.7K ohm
44	10-5332	1	" " " " 3.3K ohm
45	10-5472	1	" " " " 4.7K ohm
46	10-5103	7	" " " " 10K ohm
47	10-5333	2	" " " " 33K ohm
48	10-5473	5	" " " " 47K ohm
49	10-5104	2	" " " " 100K ohm
50	10-5564	1	" " " " 560K ohm
51	10-5125	1	" " " " 1.2M ohm
52	19-311104	1	Trimpot, 100K, CTS #X201R104B
53	19-311105	1	Trimpot, 1M, CTS #X201R105B
54	28-101101	1	Capacitor, Dipped Mica, 100pf
55	28-101271	1	Capacitor, Dipped Mica, 270pf
56	27-101102	2	Capacitor, Ceramic Disc, .001uf
57	27-101103	3	Capacitor, Ceramic Disc, .01uf, +80%, -20%
58	27-101104	16	Capacitor, Ceramic Disc, .1uf, +80%, -20%
59	24-100105	2	Capacitor, Electrolytic, 1uf, 10V
60	24-100106	4	Capacitor, Electrolytic, 10uf, 10V
61	24-250107	1	Capacitor, Electrolytic, 100uf, 25V
62	24-250227	1	Capacitor, Electrolytic, 220uf, 25V
63	24-060257	1	Capacitor, Electrolytic, 250uf, 6V
64	24-160507	1	Capacitor, Electrolytic, 500uf, 16V
65	24-250478	1	Capacitor, Electrolytic, 4700uf, 25V
66	21-101104	1	Capacitor, Mylar, 0.1uf, 10%
67	31-1N914	11	Diode, 1N914
68	31-1N4001	3	Diode, 1N4001
69	32-1N4742	1	Diode, Zener, 1N4742
70	34-2N3643	3	Transistor, NPN, 2N3643
71	33-2N3644	3	Transistor, PNP, 2N3644
72	002743	1	Crystal, 12.096 Mhz
73	66-08	1	Dip Switch, Molex 4130, #01-70-0106
74	003212	1	Printed Circuit Board



